

MFMox Ferroelectric Memory Transistor

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Abstract

In spite of extensive study of the ferroelectric memory transistors during the past 10 years the device is still far away from practical use. The charge retention time of the current version of ferroelectric memory transistor is no longer than one month. The short charge retention in ferroelectric memory transistor is mainly caused by the floating gate and the gate insulator. The gate insulator induced a relatively large field to the ferroelectric thin film even when the gate electrode is grounded during standby condition. The field across the ferroelectric thin film reducing the polarization of the ferroelectric thin film at the mean time caused current flow through the ferroelectric thin film. The standby current caused the accumulation of charges at the floating bottom electrode which in turn compensate the polarization charge.

We present an alternative device structure to solve this problem. The gate structure of the new ferroelectric memory transistor is Metal on ferroelectric on bottom electrode on semiconductive metal oxide on silicon. The bottom electrode is in direct contact to the semiconductive metal oxide. Therefore, there is no floating gate in this device. It can be shown that there can be no standby field across the ferroelectric when the device is programmed to the "OFF" state and that the standby field across the ferroelectric is fairly small when the device is programmed to the "ON" state. We will present the experimental data of the electrical property and the charge retention of the devices. The memory window, defined as $V_{TH}-V_{TL}$, extrapolated from 4 days of measurement data to 10 years is about 1V as is shown in the figure below.

